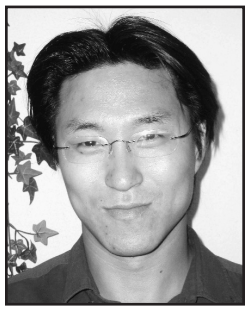
Session 20 Overview

TD: Proximity Data and Power Transmission



Chair: Chris Van Hoof, *IMEC, Leuven, Belgium*

Associate Chair: Philippe Royannez, *Texas Instruments, Villeneuve Loubet, France*

To allow for increasingly complex system functionalities, electronic systems are also becoming more-and-more heterogeneous in their technology buildup. Specific technologies (e.g., logic, memory, analog, mixed-signal, RF, MEMS) need to be integrated in a very small footprint. 3D integration is a key technology to achieve this heterogeneous integration as well as dramatic size reduction.

A new class of 3D-integrated systems is emerging that relies on contactless coupling between dice in close proximity. Such an approach puts fewer constraints on the integration technology. This coupling can be achieved by inductive as well as by capacitive coupling. While continuous progress is being made, size of proximity interconnects and power consumption overhead still are critical factors.

This session presents significant advances in terms of size and power reduction of inductive and capacitive coupling (Papers 20.1, 20.2, 20.3 and 20.7). Capacitive coupling with an energy consumption of 0.08pJ/b and a throughput of more than 22Mb/s/μm^2 is demonstrated in an array of 104 8x8μm^2 electrodes, in Paper 20.1 from ARCES, STMicroelectronics and Fraunhofer IZM. Inductive coupling at 1Gb/s/channel with energy consumption of 0.14pJ/b is demonstrated in Paper 20.2 from Keio U and U Tokyo. Paper 20.3 from Keio U and Renesas presents how this technology can be applied effectively to achieve proximity probing of logic circuits at a distance of 1.2mm and a maximum data rate of 20Mb/s. Paper 20.7 from Sun Microsystems presents a capacitively-coupled I/O link with 144 channels that operates at 1.8Gb/s/channel.

Apart from data transmission, power can also be provided. Paper 20.4 from U Tokyo and Kobe U presents advances in a contactless power delivery sheet with 50% power transmission efficiency as an enabler for wireless sensor networks and ambient intelligence. A key advance is an organic level-shifter from 5V to 40V so digital LSI logic can drive the organic FETs.

The next two papers of the session concentrate on ultra-low-power communication in a Body-Area Network environment. In Paper 20.5, from National Chiao-Tung U, an ultra-low-power wireless sensor node consuming 21μW and a central processing node consuming 566.4μW is demonstrated in a 10 sensor node configuration and is based on Multi-Tone CDMA with front-end calibration. By designing a scalable body-coupled transceiver in 0.18μm CMOS, Paper 20.6, from KAIST, achieves communication at up to 10Mb/s over the shared body channel at a reception bit-energy of the transceiver of 0.19nJ/b.

20.1 3D Capacitive Interconnections with Mono- and Bi-Directional Capabilities **1:30 PM**

R. Canegallo, STMicroelectronics FTM, Agrate Brianza, Italy

A wireless interconnection scheme based on capacitive coupling provides mono- and bi-directional transmission capabilities for 3D system integration. Chips are implemented in 0.13µm CMOS and assembled face-to-face. RX-TX circuits are connected by 8×8µm^2 electrodes and this enables the vertical propagation of clock at 1.7GHz, a propagation delay of 420ps for general purpose signals and a throughput of more than 22Mb/s/µm^2 with 0.08pJ/b energy consumption.

20.2 A 0.14pJ/b Inductive-Coupling Inter-Chip Data Transceiver with Digitally-Controlled Precise Pulse Shaping **2:00 PM**

N. Miura, Keio University, Yokohama, Japan

A transceiver for inductive-coupling is realized. By using a pulse-shaping circuit, the transmitter energy is 0.11pJ/b. Due to device scaling from 180nm CMOS to 90nm CMOS, the receiver energy is 0.03pJ/b. The overall energy dissipation is 20× lower than previous work, without degrading the data rate of 1Gb/s.

20.3 An Attachable Wireless Chip-Access Interface for Arbitrary Data Rate Using Pulse-Based Inductive-Coupling through LSI Package **2:30 PM**

H. Ishikuro, Keio University, Yokohama, Japan

A wireless logic-probing system is presented as one of the applications of the millimeter-range carrierless inductive-coupling technique. A pulse transceiver for a wireless probe and its target LSI is fabricated using a 0.25µm standard CMOS logic process. A maximum data rate of 20Mb/s and a communication range of 1.2mm is achieved.

20.4 Design Solutions for a Multi-Object Wireless Power Transmission Sheet Based on Plastic Switches **3:15 PM**

M. Takamiya, University of Tokyo, Tokyo, Japan

Design innovations that solve shortcomings of a wireless power transmission sheet are presented. The sheet is made with plastic MEMS switches and organic FET circuits. By using a level shifter with adaptive biasing in the organic circuit, the sheet can be directly driven using 5V digital input. It delivers power to multiple objects, frees the user from position adjustment, and reduces the number of coil arrays.

20.5 A Sub-mW Multi-Tone CDMA Baseband Transceiver Chipset for Wireless Body Area Network Applications **3:45 PM**

J-Y. Yu, National Chiao-Tung University, Hsinchu, Taiwan

A 0.13µm CMOS chipset containing both a wireless sensor node (WSN) and central processing node (CPN) is designed for a wireless body area network. The multi-tone CDMA scheme uses front-end calibration to improve system performance and duty-cycle control to reduce power dissipation. This system allows 10 sensor nodes to coexist and dissipates 21µW(WSN) and 566.4µW(CPN) at 143kb/s and 0.8V supply.

20.6 A 0.9V 2.6mW Body-Coupled Scalable PHY Transceiver for Body Sensor Applications **4:15 PM**

S-J. Song, KAIST, Daejeon, Korea

An energy-efficient scalable PHY transceiver for body-coupled communications is presented. The analog front-end exploits pulse detection and cross-delayed sampling techniques. The digital baseband has a hierarchical block gating architecture for energy-efficient packet processing. The 0.18µm CMOS PHY transceiver chip operates up to 10Mb/s while consuming 2.6mW from a 0.9V supply.

20.7 Circuit Techniques to Enable 430Gb/s/mm^2 Proximity Communication **4:45 PM**

D. Hopkins, Sun Microsystems, Menlo Park, CA

Two chips communicate over a capacitively-coupled I/O link at 1.8Gb/s/ch. Channels are placed on a 36µm pitch. 144 channels operate simultaneously for an aggregate bandwidth of 260Gb/s, or 430Gb/s/mm^2 in 0.18µm CMOS. Measured energy consumption is 3.0pJ/b and BER is <10^{-15}. Electronic alignment and crosstalk rejection allow reliable I/O for practical implementation.